UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/661,486	09/14/2000	Theodore Calderone	AGLE0008	9235

22862 7590 10/18/2004

GLENN PATENT GROUP
3475 EDISON WAY, SUITE L
MENLO PARK, CA 94025

EXAMINER	
PHAN, MAN U	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/661,486	CALDERONE ET AL.	
	Examiner	Art Unit	
	Man Phan	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,17 and 18* is/are rejected.

7)☒ Claim(s) *3-7 and 19-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The application of Calderone et al. for an "N-way demultiplexer" filed 09/14/2000 has been examined. Responsive to the restriction requirement filed on 03/09/2004, affirmation of the election has been made by applicant, and a provisional election was made without traverse to prosecute the invention of group I, claims 1-7 and 17-23. Claims 8-16 and 24-32 are withdrawn from further consideration by the Examiner, 37 C.F.R. ' 1.142(b), as being drawn to a non-elected invention. Claims 1-7 and 17-23 are pending in the application.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Reference character (21) as shown in Fig. 2.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

The status of the related application USSN# noted on page 1, line 22 need to be updated.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The disclosure is objected to because of the following informalities: The detailed description of the Figs. 3 & 4 not included. Appropriate correction is required.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it contains more than 150 words, and is not limited to a single paragraph on a single sheet. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC ' 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 1038 and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-2 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (US#6,184,808) in view of Takahashi et al. (US#5,210,754).

With respect to claims 17-18, both Nakamura (US#6,184,808) and Takahashi et al. (US#5,210,754) disclose a novel system for distributing highdata rate output data to a plurality of output channels, according to the essential features of the claims. Nakamura (US#6,184,808) discloses a parallel-to-parallel converter for converting an "m"-bit parallel signal into an "n"-bit parallel signal, a common multiple register has a bit width which is a common multiple of "m" and "n". An input selector is connected to an input of the common multiple register, and writes the "m"-bit parallel signal into the common multiple register at a predetermined frequency. An output selector is connected to an output of the common multiple register, and reads the "n"-bit parallel signal from the common multiple register at a frequency equal to m/n times the

predetermined frequency (Col. 1, lines 42 plus and Col. 7, lines 25 plus). Fig. 8 illustrated detailed circuit block diagrams of the parallel –to-parallel converter of Fig. 7, in which the 8-to-10 converter 204 is constructed by a clock signal generation circuit 4 in addition to the common multiple register 1, the input selector 2 and the output selector 3 of Fig. 6. The input selector 2 includes an input register 21 for temporarily holding 8-bit data (500 MHz) to be stored in the common multiple register 1. Also, the output selector 3 includes an output register 31 for temporarily holding 10-bit data (400 MHz) output from the common multiple register 1, tri-state buffers 32-1 through 32-4 for controlling the input of the data from the common multiple register 1 to the output register 31 (Col. 5, lines 7 plus).

In the same field of endeavor, Takahashi et al. (US#5,210,754) discloses a demultiplexed pattern synchronizing circuit with which it s possible to synchronize a reference pattern with input data in a short time. Fig. 1 illustrated a pattern synchronizing circuit, in which high-speed data HD, which is a repetition of an ML sequence having a pattern length of (2.sup.n -1) bits, is provided via a digital transmission system (not shown) to a terminal 11 and is demultiplexed by a demultiplexer 15 into N parallel sequences of low-speed data on N output lines 1 to N. In this instance, the N may assume an arbitrary value which is N=2.sup.a (where a is an integer equal to or greater than 1). High-speed clocks HCL are applied to a terminal 12 in synchronization with the high-speed input data HD. The high-speed clock HCL is applied to a pre-clock eliminator 13, which normally outputs it intact but, when supplied with one clock pulse eliminating signal CT2, eliminates one clock pulse as described later on. The output clock FCL from the pre-clock eliminator 13 is divided by a divider 14 down to 1/N. The demultiplexer 15 operates as a serial-parallel converter and repeats operations of fetching the high-speed input data HD of N

consecutive bits in synchronization with N clock pulses HCL and outputting them in parallel in synchronization with one divided clock DCL. Thus the high-speed input data HD is converted to N parallel sequences of low-speed data LD.sub.1 to LD.sub.N under control of the clock HCL from the terminal 12 and the clock DCL from the divider 14 as referred to above (Col. 3, lines 58 plus).

Regarding claims 1-2, they are method claims corresponding to the apparatus claims 17-18 above. Therefore, claims 1-2 are analyzed and rejected as previously discussed with respect to claims 17-18.

One skilled in the art would have recognized the need for effectively and efficiently meditating data exchange rates among various various componentos of a distribution network utilizing demultiplexer, and would have applied Takahashi's novel use of a pattern synchronizing circuit of the demultiplexing into Nakamura' teaching of a parralell to parralell converter for converting m bit parallel signal into an n bit parallel signal. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Takahashi's pattern synchronizing circuit into Nakamura' parallel to parallel converter including common multiple register with the motivation being to provide a method and apparatus for distributing high data rate output data to a number of different ports output channels.

Allowable Subject Matter

5. Claims 3-7 and 19-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest a synchronizing scheme in which a synchronization string is always written to a particular channel before the output channels are allowed to be clocked, as expressly recited in claims 3, 19.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Shimada et al. (US#5,726,990) is cited to show the multiplexer and demultiplexer.

The Obana et al. (US#5,001,711) is cited to show the complex multiplexer/demultiplexer.

The Arvidsson et al. (US#6,009,107) is cited to show the data transmission system.

The Azami et al. (US#6,750,792) is cited to show the serial to parallel conversion circuit, and semiconductors display device employing the same.

The Ridgway (US#6,369,614) is cited to show the asynchronous completion prediction.

The Meyer et al. (US#6,668,292) is cited to show the system and method for initiating a serial data transfer between two clock domains.

The Sasaki et al. (US#5,321,400) is cited to show the serial data interface circuit dealing with a plurality of receiving modes.

The Lawrence (US#6,323,789) is cited to show the method and apparatus for combining a plurality of 8B/10B encoded data streams.

The Buhrgard et al. (US#5,604,739) is cited to show signal receiving and transmitting unit for converting a transmission rate of a received signal to a transmission rate of a transmitted signal

The Denton (US#5,923,653) is cited to show the SONET/SDH receiver processor

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Phan whose telephone number is (571) 272-3149. The examiner can normally be reached on Mon - Fri from 6:00 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

9. ***Any response to this action should be mailed to:***

Commissioner of Patents and Trademarks: Washington, D.C. 20231

or faxed to: (703) 305-9051, (for formal communications intended for entry)

Or: (703) 305-3988 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Mphan

10/06/2004.

MAN U. PHAN
PRIMARY EXAMINER